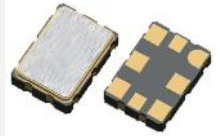


## MINIATURE CERAMIC SMD VCXO (7.0 x 5.0mm)

### FEATURES:

- Available output frequency from 15MHz to 2.1GHz
- Ultra low phase jitter <300fs
- Available LVCMOS, LVDS, LVPECL, CML, HCSL outputs
- 3.3V, 2.5V and 1.8V supply options



## ELECTRICAL SPECIFICATION

LVCMOS							
Parameter	3.3V		2.5V		1.8V		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD) ±10%	3.63	2.97	2.25	2.75	1.71	1.89	V
Frequency Range	15	250	15	250	15	250	MHz
Supply Current		90		80		70	mA
Output Level	Output High	0.9 X VDD	0.9 X VDD	0.9 X VDD	0.9 X VDD	0.9 X VDD	V
	Output Low		0.1 X VDD	0.1 X VDD	0.1 X VDD	0.1 X VDD	
Rise Time / Fall Time (20%-80%)		1.2		1.5		2.0	nSec
Duty Cycle	45	55	45	55	45	55	%
Startup Time		8		8		8	mSec
Tri-State Mode (Input to Pin 2)	Enable	0.7 x VDD	0.7 x VDD	0.7 x VDD	0.7 x VDD	0.7 x VDD	V
	Disable		0.3 x VDD	0.3 x VDD	0.3 x VDD	0.3 x VDD	
Standby Current		90		80		70	mA
Output Load				15pF			
Period Jitter		100		100		100	ps

LVPECL						
Parameter	3.3V		2.5V		Unit	
	Min.	Max.	Min.	Max.		
Supply Voltage Variation (VDD)	3.63	2.97	2.25	2.75	V	
Frequency Range	15	2100	15	2100	MHz	
Supply Current		120		95	mA	
Output Level	Output High	VDD-1.165	VDD-0.8	VDD-1.165	VDD-0.8	V
	Output Low	VDD-2.0	VDD-1.55	VDD-2.0	VDD-1.55	
Rise Time / Fall Time (20%-80%)		0.35		0.35	nSec	
Duty Cycle	45	55	45	55	%	
Startup Time		8		8	mSec	
Tri-State Mode (Input to Pin 2)	Enable	0.7 x VDD	0.7 x VDD	0.7 x VDD	V	
	Disable		0.3 x VDD	0.3 x VDD		
Standby Current		120		95	mA	
Output Load		50 ohms into VDD-2V				

Phase Noise	3.3V		2.5V		
	Typ.	Max.	Typ.	Max.	
At VDD=3.3V , Fout=644.5MHz	1kHz offset	-87	-87		dBc/Hz
	10kHz offset	-110	-110		
	100kHz offset	-127	-127		
	1MHz offset	-138	-138		
	20MHz offset	-153	-153		
RMS Phase Jitter (12kHz to 20MHz)	250	300	250	300	fs
Period Jitter		50		50	ps

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LVDS							
Parameter	3.3V		2.5V		1.8V		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)	3.63	2.97	2.25	2.75	1.71	1.89	V
Frequency Range	15	2100	15	2100	15	2100	MHz
Supply Current		90		80		70	mA
Output Level	Output High	1.6		1.6		1.6	V
	Output Low	0.9	0.9		0.9		
Rise Time / Fall Time (20%-80%)		0.35		0.35		0.35	nSec
Duty Cycle	45	55	45	55	45	55	%
Startup Time		8		8		8	mSec
Tri-State Mode (Input to Pin 2)	Enable	0.7 x VDD	0.7 x VDD		0.7 x VDD		V
	Disable		0.3 x VDD	0.3 x VDD		0.3 x VDD	
Standby Current		90		80		70	mA
Output Load	100 ohms between OUT and OUTN						

Phase Noise		3.3V		2.5V		1.8V		Unit
		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=3.3V, Fout=644.5MHz	1kHz offset	-87		-87		-87		dBc/Hz
	10kHz offset	-110		-110		-110		
	100kHz offset	-127		-127		-127		
	1MHz offset	-138		-138		-138		
	20MHz offset	-153		-153		-153		
RMS Phase Jitter (12kHz to 20MHz)		250	300	250	300	250	300	fs
Period Jitter			50		50		50	ps

CML								
Parameter	3.3V		2.5V		1.8V		unit	
	Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (VDD)	3.63	2.97	2.25	2.75	1.71	1.89	V	
Frequency Range	15	2100	15	2100	15	2100	MHz	
Supply Current		90		80		70	mA	
Output Level	Output High	VDD-0.085	VDD	VDD-0.085	VDD	VDD-0.085	VDD	V
	Output Low	VDD-0.6	VDD-0.32	VDD-0.6	VDD-0.32	VDD-0.6	VDD-0.32	
Rise Time / Fall Time (20%-80%)		0.35		0.35		0.35	nSec	
Duty Cycle	45	55	45	55	45	55	%	
Startup Time		8		8		8	mSec	
Tri-State Mode (Input to Pin 2)	Enable	0.7 x VDD	0.7 x VDD		0.7 x VDD		V	
	Disable		0.3 x VDD	0.3 x VDD		0.3 x VDD		
Standby Current		90		80		70	mA	
Output Load	50 ohms to VDD							

Phase Noise		3.3V		2.5V		1.8V		Unit
		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=3.3V, Fout=644.5MHz	1kHz offset	-87		-87		-87		dBc/Hz
	10kHz offset	-110		-110		-110		
	100kHz offset	-127		-127		-127		
	1MHz offset	-138		-138		-138		
	20MHz offset	-153		-153		-153		
RMS Phase Jitter (12kHz to 20MHz)		250	300	250	300	250	300	fs
Period Jitter			50		50		50	ps

HCSL								
Parameter	3.3V		2.5V		1.8V		Unit	
	Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (VDD)	3.63	2.97	2.25	2.75	1.71	1.89	V	
Frequency Range	15	700	15	700	15	700	MHz	
Supply Current		115		100		94	mA	
Output Level	Output High	0.66	1.15	0.66	1.15	0.66	1.15	V
	Output Low	0	0.15	0	0.15	0	0.15	
Rise Time / Fall Time (20%-80%)		0.4		0.4		0.4	nSec	
Duty Cycle	45	55	45	55	45	55	%	
Startup Time		8		8		8	mSec	
Tri-State Mode (Input to Pin 2)	Enable	0.7 x VDD		0.7 x VDD		0.7 x VDD	V	
	Disable		0.3 x VDD		0.3 x VDD			0.3 x VDD
Standby Current		115		100		95	mA	
Output Load	50 ohms to GND							

Phase Noise		3.3V		2.5V		1.8V		Unit
		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=3.3V, Fout=644.5MHz	1kHz offset	-87		-87		-87		dBc/Hz
	10kHz offset	-110		-110		-110		
	100kHz offset	-127		-127		-127		
	1MHz offset	-138		-138		-138		
	20MHz offset	-153		-153		-153		
RMS Phase Jitter (12kHz to 20MHz)		250	300	250	300	250	300	fs
Period Jitter			50		50		50	ps

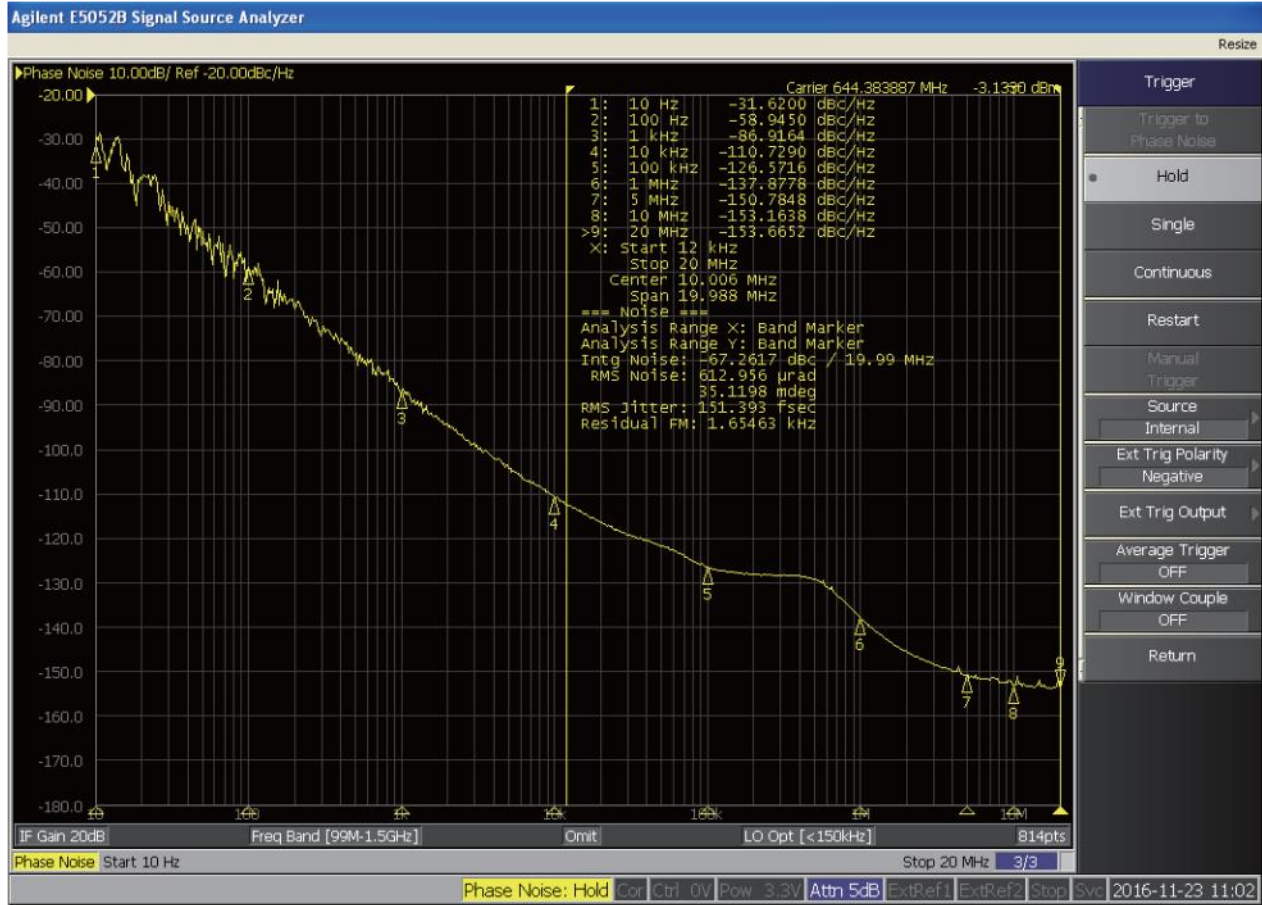
## FREQUENCY STABILITY

Parameter	Min.	Max.	Unit	Notes
Frequency Stability	±25	±100	ppm	Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year). Please select from Part Numbering Guide
Operating Temperature	-40°	+85°	C	Please select from Part Numbering Guide

## CONTROL VOLTAGE FUNCTION

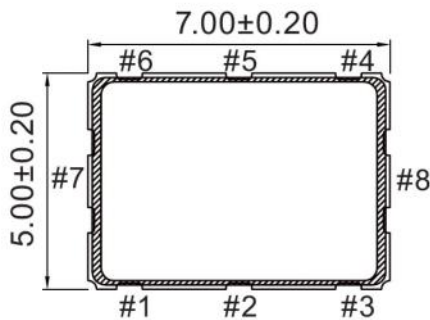
Parameter	3.3V		2.5V		1.8V		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
Center Voltage	1.65		1.25		0.9		V
Control Voltage Range	0.3	3.0	0.25	2.25	0.18	1.62	V
Pull Range	±50	±250	±50	±250	±50	±250	ppm
Linearity		±10		±10		±10	%
Modulation Bandwidth	5	20	5	20	5	20	KHz
VC Input Impedance	5		5		5		MΩ

**TYPICAL PHASE NOISE PERFORMANCE**

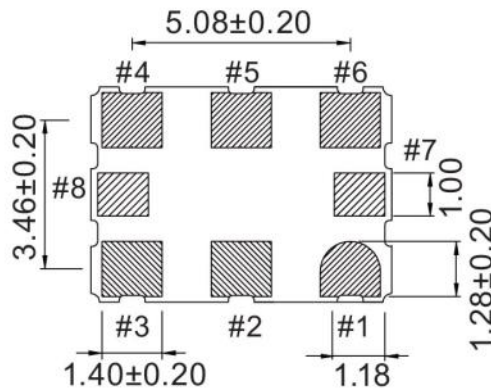


**DIMENSIONS**

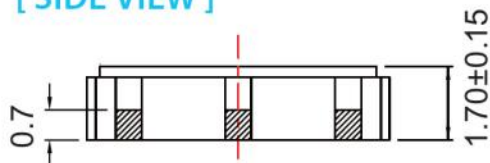
[ TOP VIEW ]



[ BOTTOM VIEW ]



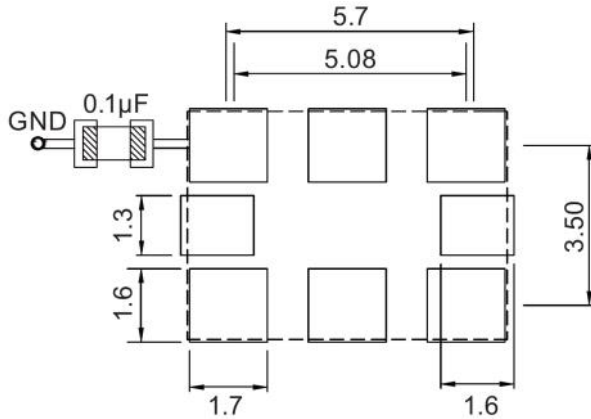
[ SIDE VIEW ]



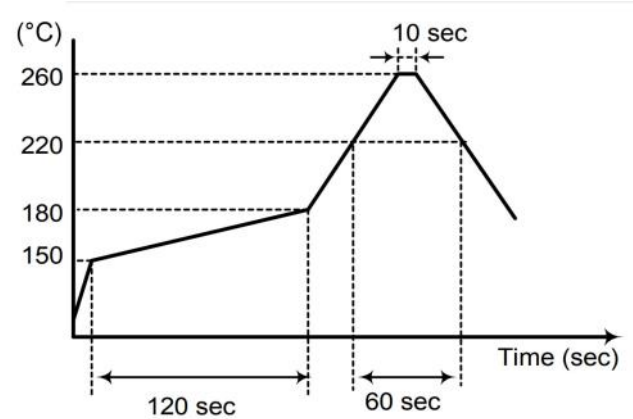
**Pin Configuration**

	LVPECL LVDS CML HCSL	LVC MOS
1	V Con	V Con
2	OE	OE
3	GND	GND
4	OUTPUT	OUTPUT
5	C. OUTPUT	NC
6	VDD	VDD
7	NC	NC
8	NC	NC

## SOLDER PATTERN



## REFLOW PROFILE



## PART NUMBERING GUIDE

